

CoWare Customer Success

STMicroelectronics Slashes Software Tool Development Time by 4X to 5X Using CoWare Processor Designer Automated Embedded Processor Design Environment

Customer Profile

The Compiler Group of STMicroelectronics' Consumer and Micro Group (CMG) develops software development environments for CMG's processors targeted at applications such as Imaging, Set Top Box, Digital TV and Digital Video Disc.

Business Challenge

CMG's overall business challenge is to deliver new processor designs and their variants with the machine gun rapidity demanded by consumer markets. The Compiler Group's challenge is to deliver the requisite processor software development tools to CMG's product divisions on time, every time, to meet CMG's stringent time to market requirements. The high introduction rate of CMG's processors mandates the use of a high productivity tool development methodology.

Design Objectives

The design objective was to rapidly generate software tools for ST's SLIM Core DMA engine in parallel with the development of the SLIM Core itself.

Results

Using CoWare Processor Designer, the Compiler Group developed the complete software toolset with one engineer-month of effort. The evolving nature of the processor's architecture necessitated toolset iterations, most of which required less than a day to execute. Overall, the Compiler Group estimates that Processor Designer reduced tool development time by 4X to 5X, and post-development maintenance effort by 10X.

The methodology enables tool development and maintenance by one engineer, rather than by a multi-disciplinary team consisting of a processor engineer for ISS design, and individual development engineers for each tool and for the compiler. Consequently, it eliminates the time-consuming necessity to integrate components and tools from multiple design sources, which often use different specifications and disparate tools to develop the requisite components.

"Using CoWare Processor Designer, we developed the complete software toolset for our SLIM Core DMA engine with only one engineer-month of effort. We then delivered a further 15 variants in response to processor architecture changes and evolving customer requirements. It now takes longer to modify release notes with tool update information than to update the tools and re-generate them for three host operating systems"

– Christian Bertin,
Manager of the Compiler Group of
ST's Consumer and Micro Group.

CoWare Processor Designer Adoption

The Compiler Group evaluated Processor Designer for its ability to meet the Group's established automated methodology requirements, including:

- Integrated environment to ensure consistency between architecture models, instruction set simulator (ISS) and software development tools.
- Fast model creation to support rapid architectural exploration and tool generation for multiple variants.
- Single "golden source" for all models to ensure model compatibility and "correct by construction" results.
- Automatic generation of validated instruction accurate ISS for software execution of target programs – e.g. for ST200 – on a host system such as SPARC/Solaris.
- Automatic generation of cycle-accurate ISS to tune system performance via observation of pipeline and memory activity, and to validate the RTL implementation.
- Fast ISS execution to speed compiler validation with very large industrial test suites, to validate the tool suite, and to bootstrap OS kernels.
- Easy distribution of software tools, and easy installation by engineers without expert knowledge thereof.

The Compiler Group integrated CoWare Processor Designer into its software development tool flow, illustrated below, using the ST220 32-bit VLIW processor as a testbed. The Group started by creating an architectural model of the ST220 in the LISA language, and verified it against ST's existing ST220 "golden" model. The Group then used Processor Designer to generate an instruction-accurate ISS that, using its Just-in-Time Cache Compiled (JIT-CC™) simulation, executed an order of magnitude faster than the existing ISS. The whole process took less than four weeks elapsed time. The Processor Designer ISS was then used to validate the ST220 compiler that the Compiler Group had already developed.

Following this successful evaluation, the Group applied the Processor Designer-enabled methodology to the ST SLIM Core design. The architectural model, assembler, linker, debugger, profiler, pipeline and memory analysis tool, custom host loader and instruction-accurate ISS were generated within 6 weeks with 1 engineer-month of effort.

Because the SLIM Core was itself undergoing design changes, the Group was required to generate new development tools for each design iteration. Processor Designer enabled the Group to quickly develop and deliver no fewer than fifteen toolset variants to the client product division, on time. Using the traditional development methodology, this would have required the development of a point tool for each variant, with significant time delays.

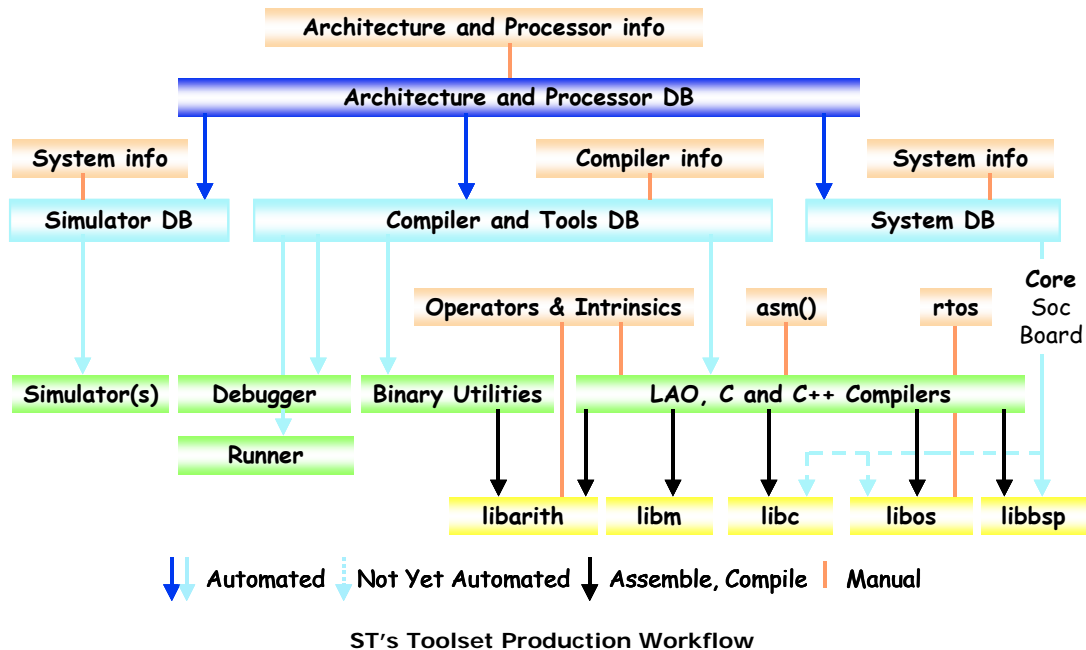
The Compiler Group has since used CoWare Processor Designer to develop instruction-accurate ISS for the ST5, ST7, STM7, and MSC1 processors. Moreover, the Group has developed an automated CHESS-to-PD flow, enabling it to automatically generate simulators for processors designed using ST's own CHESS processor description language and database structure – such as the ST7 and STM7 – that undergo occasional modification.

Conclusion

CoWare Processor Designer satisfied CMG's requirements for an automated development methodology, delivering dramatic improvements in design productivity; fast execution; consistent models; and "correct by construction" ISS and tools. Using CoWare Processor Designer, ST slashed the time to develop processor-specific software tools by 4X–5X in parallel with multiple processor design iterations.

CoWare Processor Designer's automated solution enables ST to develop software tools not only for significantly more processor types with application- and market-specific variants than was previously possible, but also for processor designs in progress. Furthermore, recent Processor Designer innovations have reduced tool build time from 1 day to 30 minutes.

CoWare Processor Designer is now an indispensable engine in CMG's software tool development flow.



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