

CoWare Customer Success

Achieving a Successful ESL Design Methodology Transition: How CoWare Services Helped Toshiba Information Systems (Japan) Corp. to become a “Total Solution Provider”

Toshiba Information Systems’ Embedded Solutions Group

The embedded systems for information equipment such as cellular phones, household information devices and in-vehicle information equipment are becoming increasingly sophisticated. The Embedded Solutions Group of Toshiba Information Systems (Japan) Corporation (TJ) provides state-of-the-art solutions including platform and application development. This group also provides SoC total solutions, from support for embedded application software design, middleware development and porting, driver design and development to consultation. The Embedded Solutions Group includes an LSI Solutions Division. The development of system LSIs is essential to the latest IT such as home electronics information appliances, network terminals and mobile communication. The LSI Solutions Division is comprehensively engaged in semiconductor system design, logic design, circuit design, layout design, LSI development, support tools, evaluation and analysis and board and firmware development.

The LSI Solutions Division’s Business Challenge

The LSI Solutions Division’s General Manager, Mr. Yasuyoshi Kodama, had noticed that the current embedded systems designs were becoming considerably more complex and had much higher performance requirements than was previously the case. Software, firmware and LSI hardware all needed to be faster. Specifically for LSI design, introduction of new nanometer processes was driving SoC’s of such complexity that they were becoming very difficult to verify with the existing methodology based on RTL simulators. Additionally, system-level design

decisions, such as hardware-software partitioning and finding the optimal architecture, were being taken based on “guru knowledge” – estimates based on the architects’ experience of previous designs. Because of the increasing complexity of the systems, architectural decisions taken on previous designs were no longer appropriate for the current designs; hence mistakes were starting to creep into the process at the system specification level.

“The training, modeling assistance, knowledge transfer and ongoing support we received from the CoWare Professional Services team was invaluable to attain maximum efficiency with our new ESL design flow in minimum time”

Takao Shijo
Group Manager
LSI Design Center

Kodama-san challenged the team to increase competitiveness in the face of this rapidly-increasing embedded systems complexity by becoming a one-stop shop for these systems. He outlined that this would involve improving capabilities in three areas: application software; platforms (meaning middleware, operating systems and driver software); and system LSI. Specifically for system LSI, he set a goal to reduce the design Turn-Around Time (TAT) (and hence design cost) by one-third.

Design Team Objectives

In order to attain the TAT goal set by Kodama-san, the LSI design team decided to introduce an Electronic System Level (ESL) design flow. The objective for this flow was to provide higher productivity and quality for embedded system LSI design via the following capabilities:

- Provide C modeling as well as RTL
- Prepare for high-level, synthesis-based design
- Verify by simulation at complete SoC level
- Improve simulation speed

Under the direction of Mr. Takao Shijo, Group Manager of System LSI Design Dept. 1, and after evaluation of the alternatives, a small team of architects and design team leaders in the LSI Solutions Division chose CoWare's ConvergenSC® as their ESL design environment to implement these flow capabilities. ConvergenSC was chosen for the following reasons:

- Support for SystemC – the standard language for Transaction Level Modeling (TLM). ConvergenSC is the leading ESL tool supporting SystemC
- Many of Toshiba's system vendor customers and other semiconductor companies have chosen ConvergenSC as their modeling environment
- ConvergenSC supports simulation with mixed abstraction levels including RTL co-simulation. Abstraction level can be changed block by block with RTL, bus cycle-accurate (BCA), TLM and Programmers View (PV) levels being selectable as appropriate.

Introducing the ESL Methodology:

The Mars Projects

Having chosen ConvergenSC, the LSI design team turned their thoughts to the task of introducing the new design flow. Realizing that transitioning to an ESL design methodology is a non-trivial exercise, TJ turned to CoWare's Professional Services team. CoWare's services team worked with Shijo-san, along with Mr. Yasuaki Kawamura, a Senior Manager, and leading designers in System LSI Design Dept. 1, to define a phased approach to the methodology roll-out within the LSI Solutions Division. Three projects were defined, named Mars 1, 2, and 3. Kawamura-san assumed the role of Program Manager, with the technical lead on the Mars 1 and 2 projects assuming the role of advisor on Mars 3, to help others take the lead, thus rolling out the methodology wider in the Division. Finally, the LSI Design Team undertook a fourth project, completely by them, to confirm successful transition of the ESL methodology. The objectives of each of the projects are briefly outlined in the following table:

Project	Objective	Methodology	Resources and Timeframe
Mars 1/2	To establish fundamental SystemC technology <ul style="list-style-type: none"> • Mars1: CoWare's ARM-based example platform • Mars2: based on TJ55000 platform 	<ul style="list-style-type: none"> • Gain platform model creation experience in ConvergenSC from CoWare example • Create BCA-level SystemC model from Verilog RTL code for in-house TJ55000 core 	1 designer 4 months work
Mars 3	Extend Mars 2 platform to a USB-based system level TLM design kit	Use ConvergenSC to: <ul style="list-style-type: none"> • Model USB 2.0 Host Controller at TLM level • Establish SystemC TLM channel modeling technology for USB and proprietary CPU buses 	3 designers 6 months
First TJ-only Project	To establish an architecture design environment based on bus analysis	TLM modeling methodology with ConvergenSC analysis API applied to: <ul style="list-style-type: none"> • Bus bridge between standard OCP TL2 channel and proprietary bus • Memory controller 	3 designers 3 months

The Mars 1 and 2 Projects

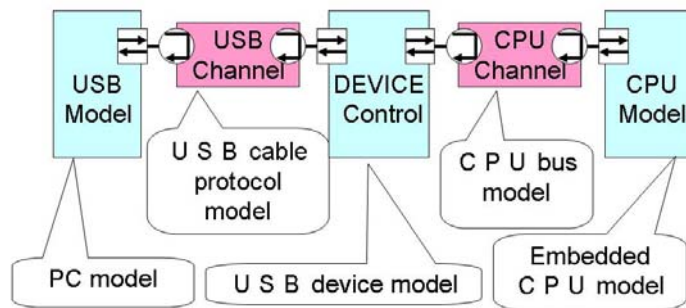
The initial Mars project kicked off with a training course on SystemC modeling and platform design in the ConvergenSC tool set. CoWare introduced the methodology for ESL design in ConvergenSC by way of a complete but simple ARM-based platform example. This example consisted of an ARM926 processor, with AMBA bus, DMA controller, ROM, RAM, SMI, Display, and input device, all modeled in SystemC at a cycle-accurate transaction level. After completing the training and familiarizing themselves with this platform to study the modeling methodology in depth, the TJ team modeled their own DMA controller at SystemC cycle-accurate TLM level, and verified it by co-simulation with the RTL. While they found the coding style at this abstraction relatively easy for an RTL designer to understand, the team was pleased to receive ongoing CoWare support during the creation of this model, which took approximately two weeks.

Next, the team embarked on the Mars 2 project. This started with a ConvergenSC workshop, delivered jointly by CoWare and the Mars 1 team, taking the findings of the Mars 1 project to a wider audience within the LSI Solutions Division. Then, the Mars 2 team created a model of the TJ55000 processor at a similar abstraction level, based on the Verilog RTL code. A bus cycle-accurate (BCA) model with transaction-level interface was created. The success criteria for the project were based on TJ satisfactorily acquiring the necessary expertise to perform this level of platform modeling by themselves, and this was completed successfully on schedule.

The Mars 3 Project

The purpose of the Mars 3 project was to create a complete, reusable ESL design kit, to enable platform architecture design in the LSI Solutions Division. The platform created in Mars 2 was extended in two main ways: by adding a USB 2.0 host controller model, with USB channel; and by adding a bus model for TJ's proprietary

CPU bus. Since creating efficient transaction-level representations of custom bus protocols can be initially challenging, CoWare helped the TJ team to create these models, in cycle-accurate TLM coding style. Once again, achieving full knowledge transfer from CoWare to the TJ team for the expertise that CoWare brought to the project was explicitly part of the success criteria. The platform is illustrated below.



The result of the Mars 3 project was to use this transaction-level SystemC Design Kit to firmly establish the SystemC-based design methodology in the LSI Solutions Division. The Mars 3 team compared specific results by running their test cases on the TLM platform and its RTL equivalent. The comparison is shown in the following table. While maintaining full cycle accuracy and showing exactly the same functional results, the SystemC TLM platform ran 10 times faster than the RTL equivalent. The TLM code was also one-fifth the number of lines compared with RTL. As well as contributing to the faster execution, this also makes the code much more easily understandable.

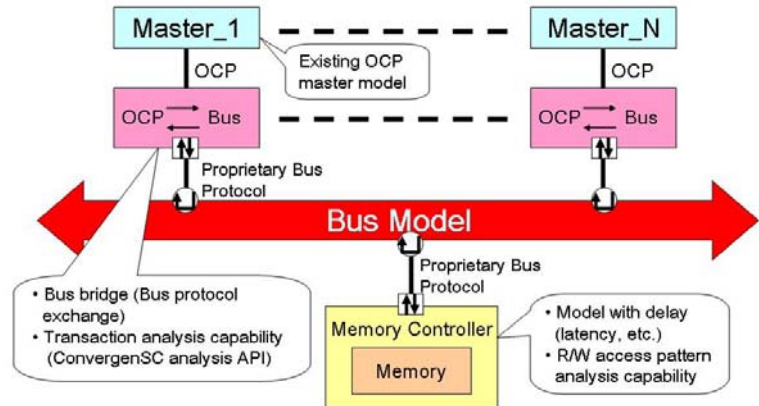
	RTL	System C
Simulation Time	500 min.	50 min.
Lines of Code	15,000 lines	3,000 lines

The First “Stand-Alone” Project

Following the success of the design kit from the Mars 3 project, the LSI Solutions Group reused the knowledge and IP models developed in the Mars projects to create a new platform for bus architecture and memory model evaluation. They created bus bridges between the Open Core

Protocol interface specification and their proprietary bus, allowing peripherals with the standard OCP interface to be easily connected. The team also created a generic memory

controller and memory model. These models were created at a higher level of abstraction than previous models – the OCP TL-2 level – which is a cycle-approximate TLM abstraction intended for faster execution for architectural exploration. The team instrumented the bus bridges and memory models using ConvergenSC’s analysis API. By annotating different cycle delays (latencies) in the memory model, the team was able to analyze different Read/Write access patterns between existing devices (OCP masters) and the memory. This platform is illustrated below.



- Prepare for high-level synthesis based design: SystemC-based modeling is suited to high-level synthesis flows, especially at the BCA level.
- Verify by simulation at complete SoC level: Higher level of abstraction, increased simulation speed, and creating TLM models for in-house processors and buses has enabled complete SoC-level verification.
- Improve simulation speed: The team achieved a ten-fold simulation speed-up at the cycle-accurate level. More dramatic speed-up can be achieved by trading some cycle accuracy and coding at higher TLM abstraction levels.

The LSI Design Team had previously found that it was difficult to implement analysis by hand, but with the TLM platform and ConvergenSC’s analysis capabilities, they managed to implement all the necessary analysis by adding just 20-30 lines to the original source code. Using this analysis capability, the team successfully managed to analyze bus utilization and determine the optimal bus architecture.

Conclusions

Through the Mars projects, TJ’s LSI Solutions Group achieved a transition to a SystemC-based ESL design methodology, and has proliferated the flow throughout an LSI design team of over 20 designers. This was achieved well within the target 12-month period by breaking the transition down into a series of digestible steps, involving progressive training to introduce first simpler, then more challenging, modeling and ESL design techniques, as represented by the Mars projects. They have fully achieved the objectives set, namely:

- Provide C modeling as well as RTL: The team has successfully adopted SystemC modeling at BCA, cycle-accurate TLM, and cycle-approximate TLM levels, as well as proving the ability to co-simulate with RTL implementations.

As for Kodama-san’s goal to reduce TAT, he states: “Working with CoWare Services to introduce our ESL design methodology has paid dividends in design efficiency. We estimate that, for equivalent complexity, we have easily exceeded our goal of one-third TAT reduction.”