

CoWare® Model Library

A Library of SystemC-based Models to Enable Electronic System Virtualization

Today's electronic system designers are tasked with the ever-increasing challenge of developing complex products and getting them to market in a minimum amount of time. To achieve these design goals, designers rely on using large amounts of Intellectual Property (IP), allowing more time for focusing on the unique value and differentiation of their product.

To enable designers to have the widest choice of IP for their product, simulation models of the IP need to be available. Models need to be of high quality, fast performance and also provide ways to ease design tasks, such as debug, and the ability to analyze performance problems.

The CoWare® Model Library is part of the CoWare solution that has been developed to address this. It contains a collection of SystemC IP models, including embedded processors, interconnects, peripherals, and memories. These models are typical of the IP needed by designers to be able to build platforms, optimize interconnect and memory subsystem architectures, debug hardware and software and verify the design before moving to the RTL implementation flow.

The models in the CoWare Model Library have been developed in partnership with major IP providers, including the market leaders ARM, IBM, MIPS, Toshiba, Tensilica, Renesas, Rambus, Sonics, CEVA and VeriSilicon, giving the designer access to IP vendor reference models and ensuring correct behavior. Other semiconductor IP partners provide models directly to the customer. For a complete listing, visit www.CoWare.com.

Embedded Processor Models

Embedded Processor Models use Instruction Set Simulators (ISS) to emulate the behavior of the implementation model. By being an

abstract representation of the RTL, the simulation performance gained is typically several orders of magnitude faster than the implementation model. This allows hardware and software designers to run more application code or more comprehensive verification suites to prove the design.

CoWare works with the designer's IP partners, using ISS models certified by the partner, ensuring that the models have the correct functionality and behavior available for SystemC simulation. Based on many years of experience, CoWare also works with many IP Partners to enable them to most efficiently create their own SystemC-compatible processor models that support features such as virtual memory, debugging and analysis to maximize the value of these models within CoWare Platform Architect, CoWare Model Designer and CoWare Virtual Platform.

With Processor Designer, CoWare not only developed a unique tool that enables customers to create dedicated and highly optimized processors (see Custom Processor Models), the tools also eases and optimizes the creation of ultra fast instruction accurate processor models. Combined with CoWare's ESV TLM methodology and the CoWare Virtual Platform technology, these ultra fast processor models enable early software development.

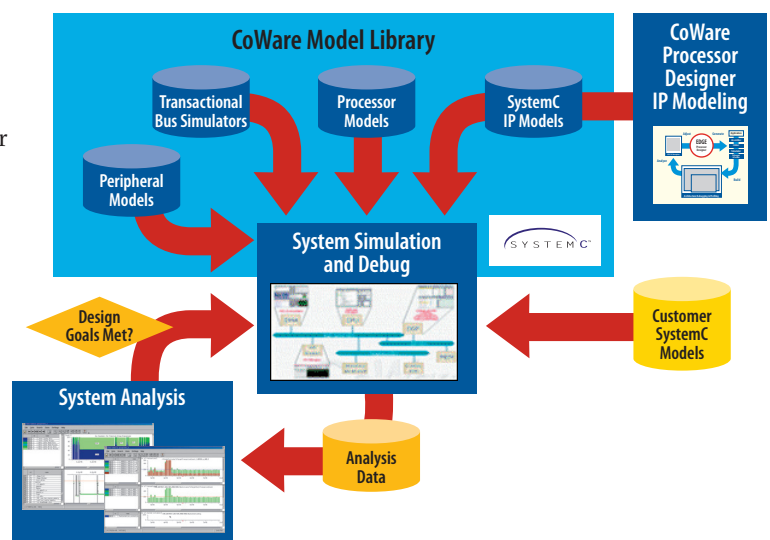
H I G H L I G H T S

- Embedded Processor Models
- Interconnect Models
- Peripheral Models
- Memory Subsystem Models
- Custom Processor Models

Interconnect Models

Whether platforms are created from scratch, or by mixing legacy blocks with newly-created functionality, it is critical that designs are easy to create, optimize and validate. CoWare's Bus Library Wizard (BL Wizard) tool capability uses Transactional Bus Simulators to automatically generate the designer's specified interconnect architecture for the platform. The resulting platform can be simulated at the transaction level for maximum simulation speed and bottlenecks can be readily identified using powerful hierarchical bus analysis.

CoWare Platform Architect combines CoWare's BL Wizard technology, tcl scripting infrastructure, unique AVF export mechanism and the industries' most comprehensive analysis infrastructure to offer an unmatched interconnect and memory



subsystem performance optimization solution for the SystemC interconnect models in the CoWare Model Library.

The bus simulators (delivered as part of a Bus Library) are available for multiple levels of abstraction and can incorporate transaction-level and RTL models, automatically building the necessary interfaces between the transaction domain and the signal domain. In this way, the designer can introduce RTL implementation models mixed into the transaction-level system one by one, resulting in huge verification performance benefits. Programmers View bus simulators are also available to dramatically increase the platform simulation performance for the purpose of running and debugging embedded software with transaction-level views of the hardware. To enable interoperability with peripherals that are developed based on CoWare's SystemC Modeling Library (SCML) at the Programmers View level, transactors are delivered with the Bus Libraries of the CoWare Model Library. The bus simulators are also compatible with the TLM2.0 standard from OSCI to enable maximum IP re-use. They support a wide variety of bus protocols including AXI, AHB, APB, OCP, PBL, DCR and OPB.

CoWare provides Bus Libraries, pre-instrumented with extensive analysis capabilities, for certain standard on-chip interconnects from ARM like ARM AMBA®, AMBA 2.0, ARM PL300 and ARM AMBA NIC-301 Network Interconnect and from other interconnect

IP vendors like Sonics and IBM. CoWare can also provide services to create bus simulators for your in-house interconnect specifications.

Peripheral Models

CoWare TLM Modeling methodology based on OSCI TLM2.0 and CoWare's SystemC Modeling Library (SCML) enables reuse of peripherals for multiple design tasks and different communication protocols. Based on this modeling methodology, CoWare has developed an extensive set of functionally accurate SystemC models for the ARM® PrimeCell® family. These models allow the designer to create and configure platforms and develop software early in the development process. On top of that CoWare delivers a Generic IP Library (GIPL) with its tools. This Generic IP Library consists of a base set of peripherals that are typically used in any platform.

Memory Subsystem Models

Memory subsystems are an increasingly important part of today's complex designs. CoWare is partnering with IP vendors like ARM, Rambus and Sonics to provide cycle accurate models of their memory controllers to feed into CoWare's interconnect and memory subsystem performance optimization solution.

An extensive range of memory models is also available through CoWare's interface to Denali's Memory Modeler-Advanced Verification

(MMAV); enabling the use of Denali models in the CoWare simulation environment.

The CoWare Model Library also provides a generic memory controller that has various timing parameters to enable mimicking various DDR and DDR2 style memory controllers for usage in CoWare's interconnect and memory subsystem performance optimization solution.

Custom Processor Models

CoWare Processor Designer allows semiconductor IP vendors or end users to rapidly create models of their processors. This includes standard RISC, DSP and Application-Specific Instruction-set Processor (ASIP) architectures.

CoWare Processor Designer automatically creates the Instruction Set Simulator (at both instruction accurate and cycle-accurate levels), from the LISA description language. All necessary software tools are generated, including assembler, disassembler, linker, profiler and debugger. Please visit www.CoWare.com for more information on CoWare Processor Designer.

IP models are continuously being added to the CoWare Model Library, please contact CoWare for the latest list of available IP and the full range of SystemC-based, electronics system virtualization design tools.

FEATURE	BENEFIT
SystemC TLM models	Spend your time on differentiating your product, not on writing IP models
Exceptional analysis & debug capabilities	Reach your product goals quicker
Pre-verified models	Simplify your design tasks, helping to reduce your time to market
TLM abstraction level of SystemC	Significantly improves simulation performance, allowing more verification to ensure right-first-time designs
RTL Bus Generators from IP vendors	Link your ESV design to implementation, reducing design errors and design time
Ultra fast processor models	Early software development in the context of the platform
Tcl scripting, AVF export and bus analysis	Rapid interconnect architecture optimization
Bridges and transactors	Platform design flexibility



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