Enablement, Evaluation and Extension of a CDM ESD Verification Tool for IC Level

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Purpose of this Work

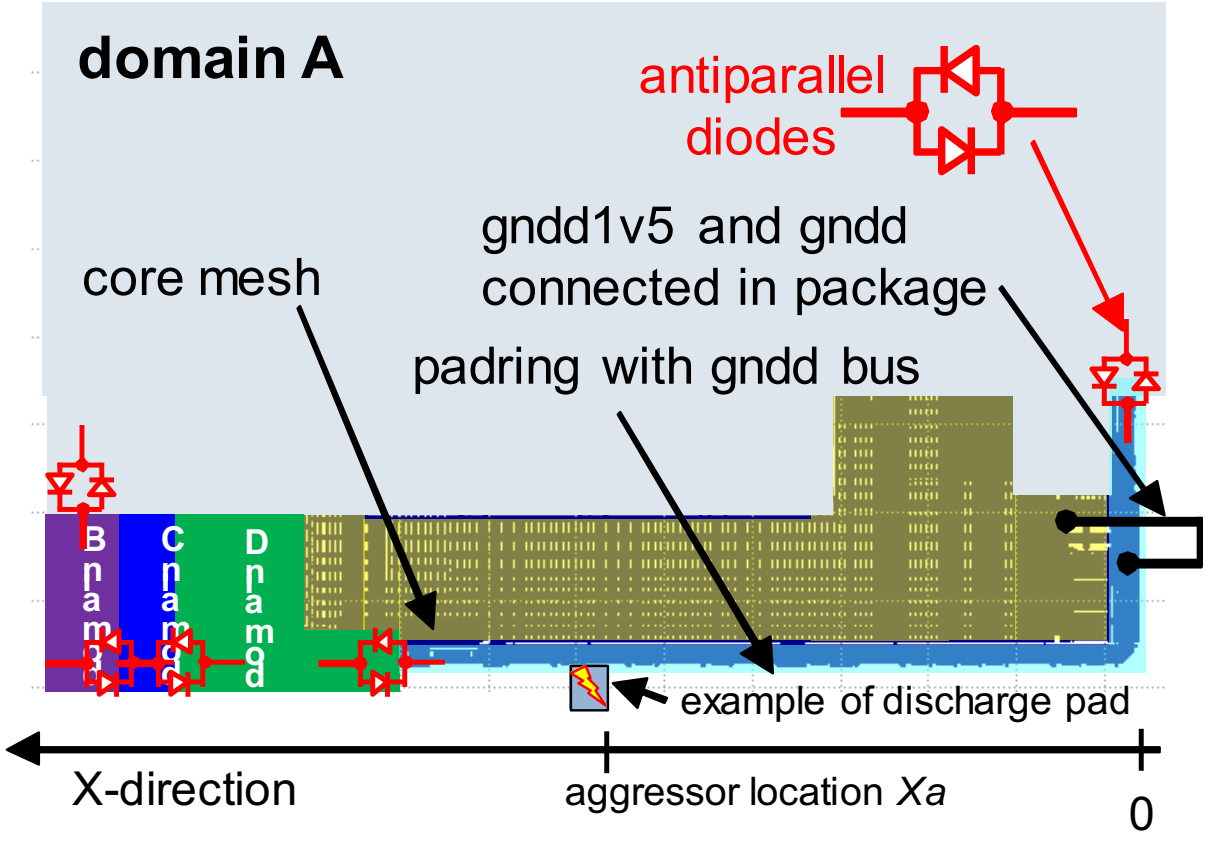
- To share experiences in enabling a CDM verification tool for IC design
- To evaluate this tool for its capability to confirm a detected physical failure
- To extend the methodology of the tool for treatment of CDM-relevant inductances
- To match pin-specific CDM-levels between tool and test results

Outline

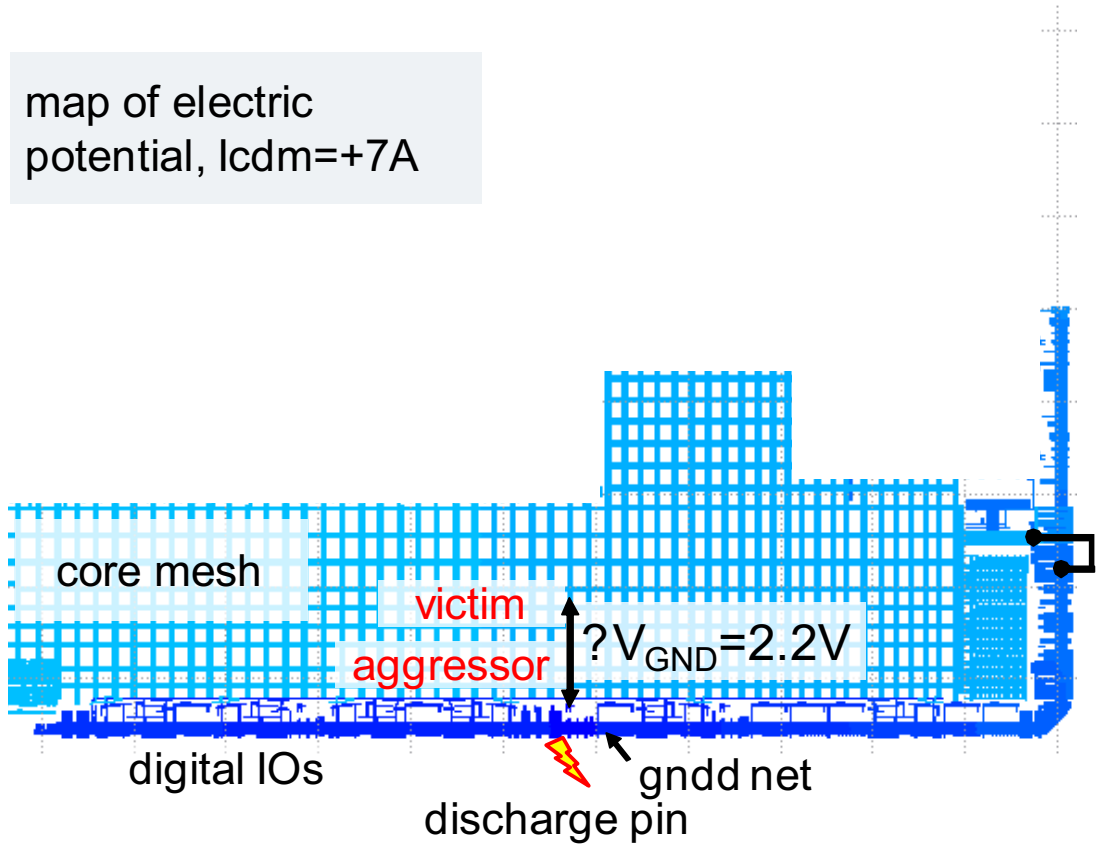
- Introduction
- Setup of CDM Verification Tool
- CDM Case Study: Bus Line Inductance
- Extended Tool Methodology: Automated Inductance Extraction
- Comparison of CDM Levels: Tool vs. Experiments
- Conclusions

Introduction (1): CDM Fails but no Explanation… ☹

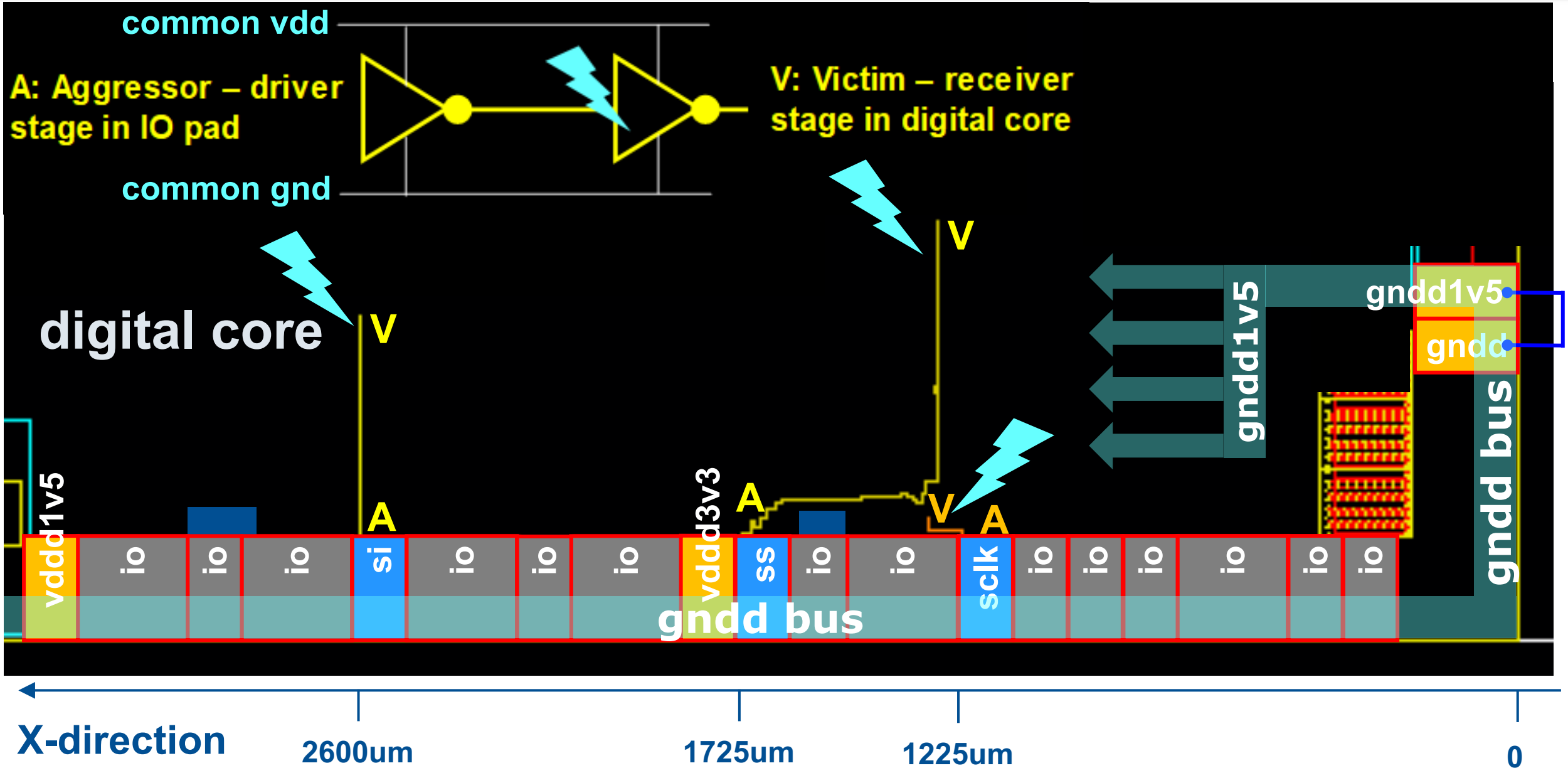
- 3-Million-transistor design, 130nm technology
- Multiple gate oxide failures observed at core RX soon above target CDM level (500V, 6A)
- Signals to RX do not cross domain border: intra-domain
- ESRA-CDM: uncritical differences in electric potential within gndd net of 2.2V



map of electric potential, Icdm=+7A



Introduction (2): Intra-Domain Interface, Aggressor vs. Victim



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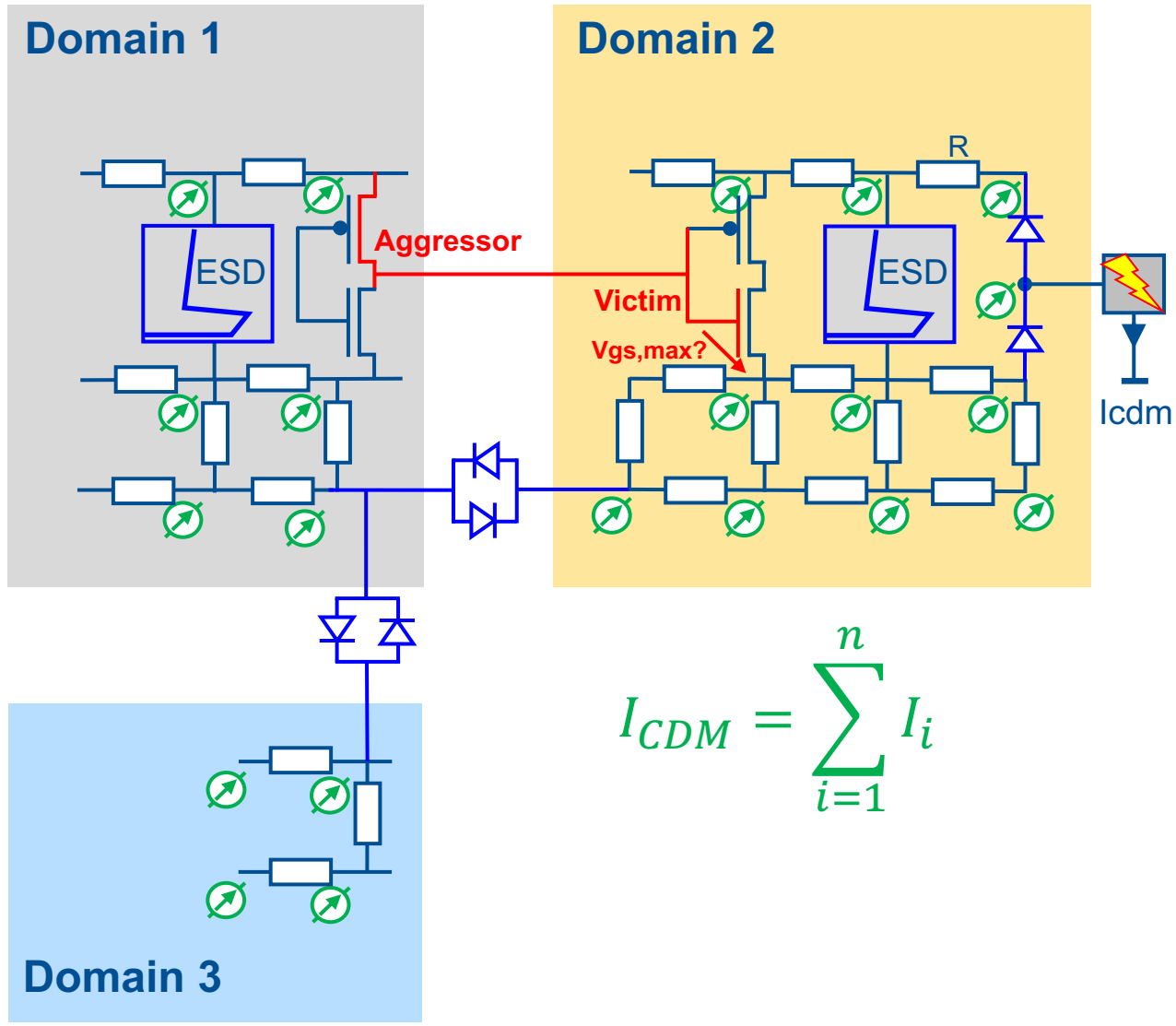
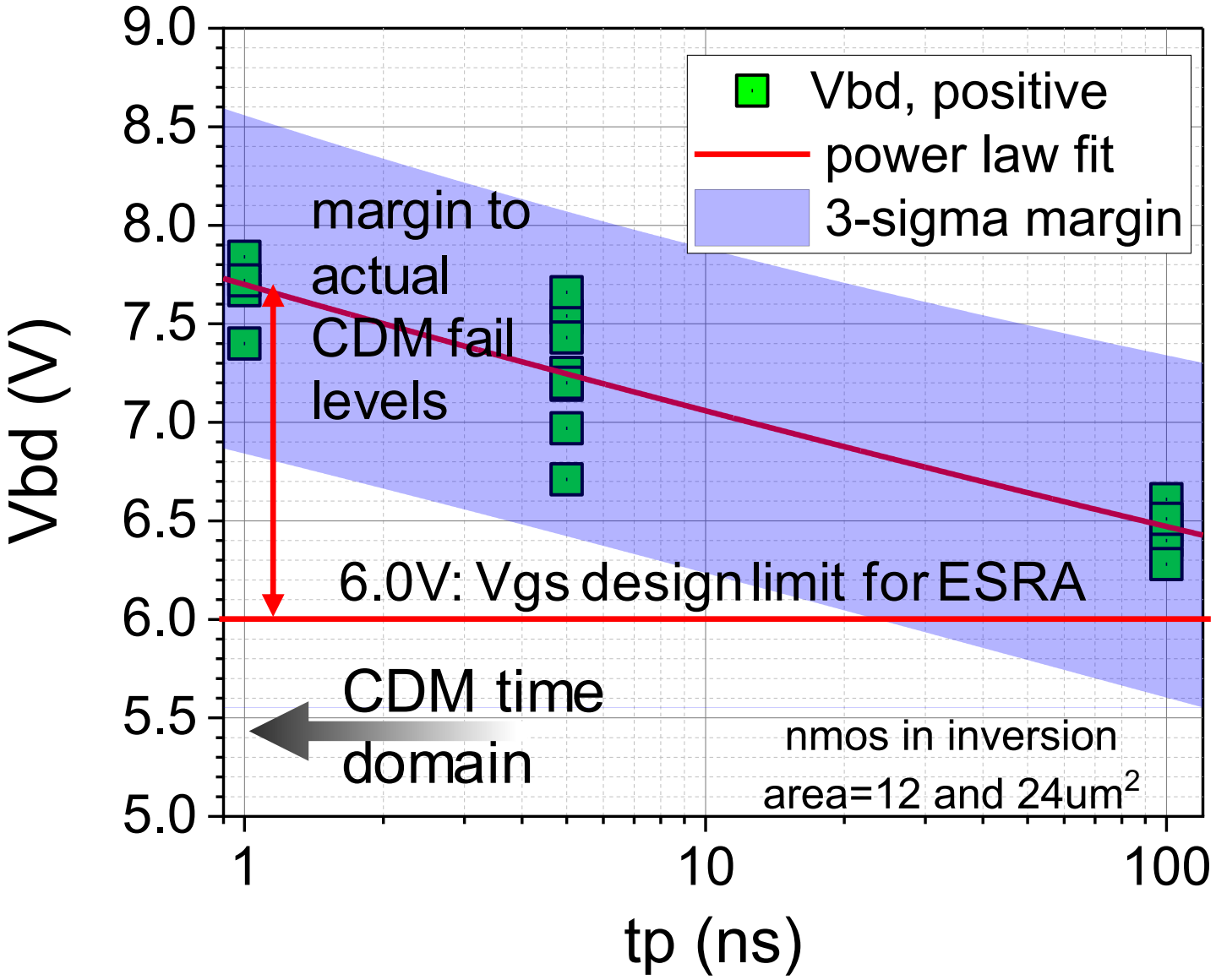
Setup and Principle of ESRA-CDM Tool

- Technology base info
- Layout (LVS-clean)
- Parasitic resistance extraction
- (vf)TLP curves of ESD elements
- Distribution of initial CDM charges according to layout area
- Circuit simulation of the ESD discharge paths
- Propagation of node voltages and comparison to limits (e.g. max Vgs) of the victims



$$I_{CDM} = \sum_{i=1}^{n} I_i$$

ESD Gate Oxide Limits for Victim Devices



- Characterization by TLP and vfTLP for tp=100ns → 1ns
- Focus on Gate-Source and Gate-Drain limits: Vgd=Vgs
- Details on measurement techniques: see full paper
- Suggested margin for design limit and actual voltage for CDM failures

- Notice a flaw in the graphic of figure 6 in the paper: 1ns data is hidden ☹

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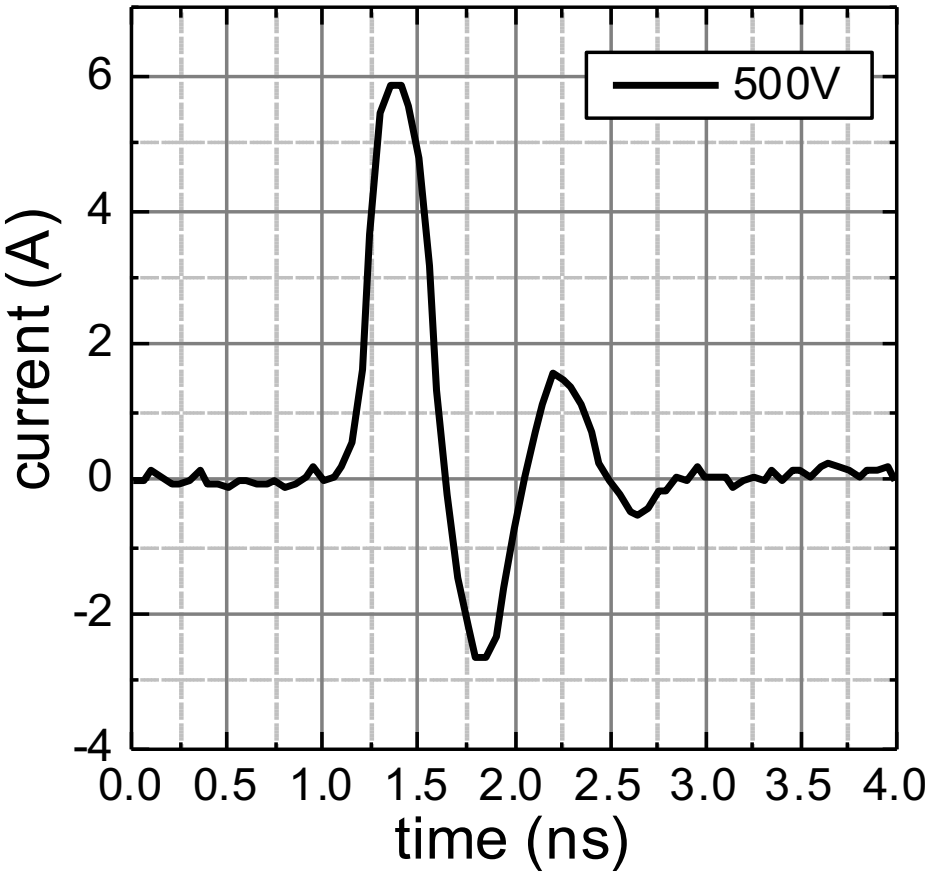
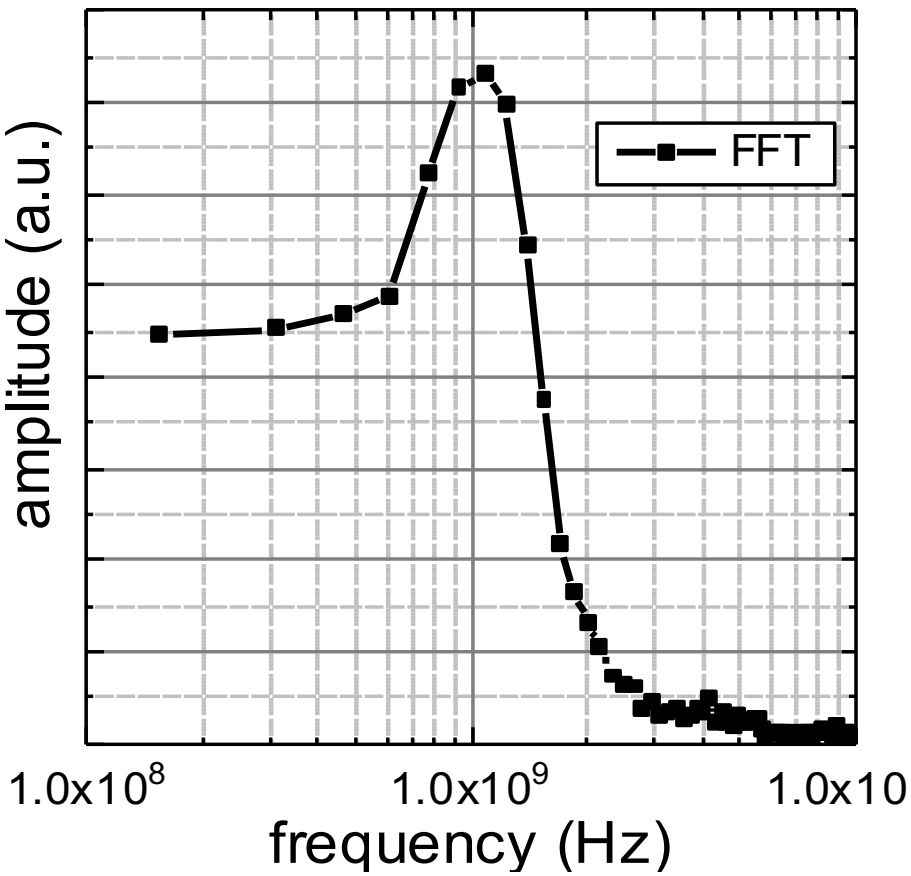
CDM Case Study

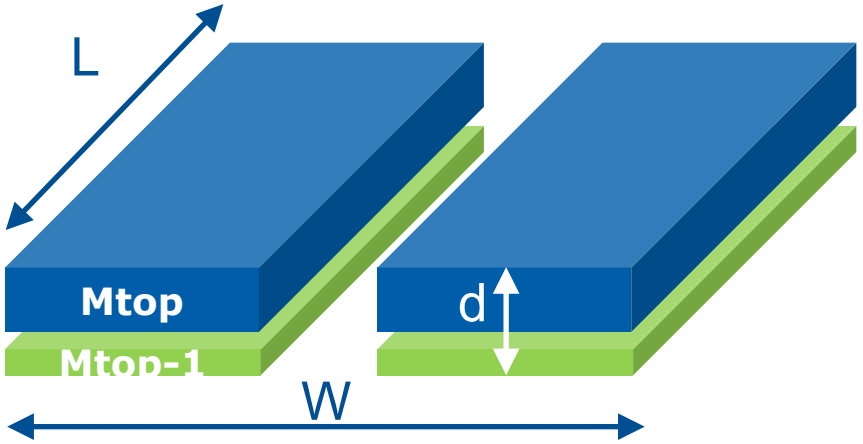


FFT →

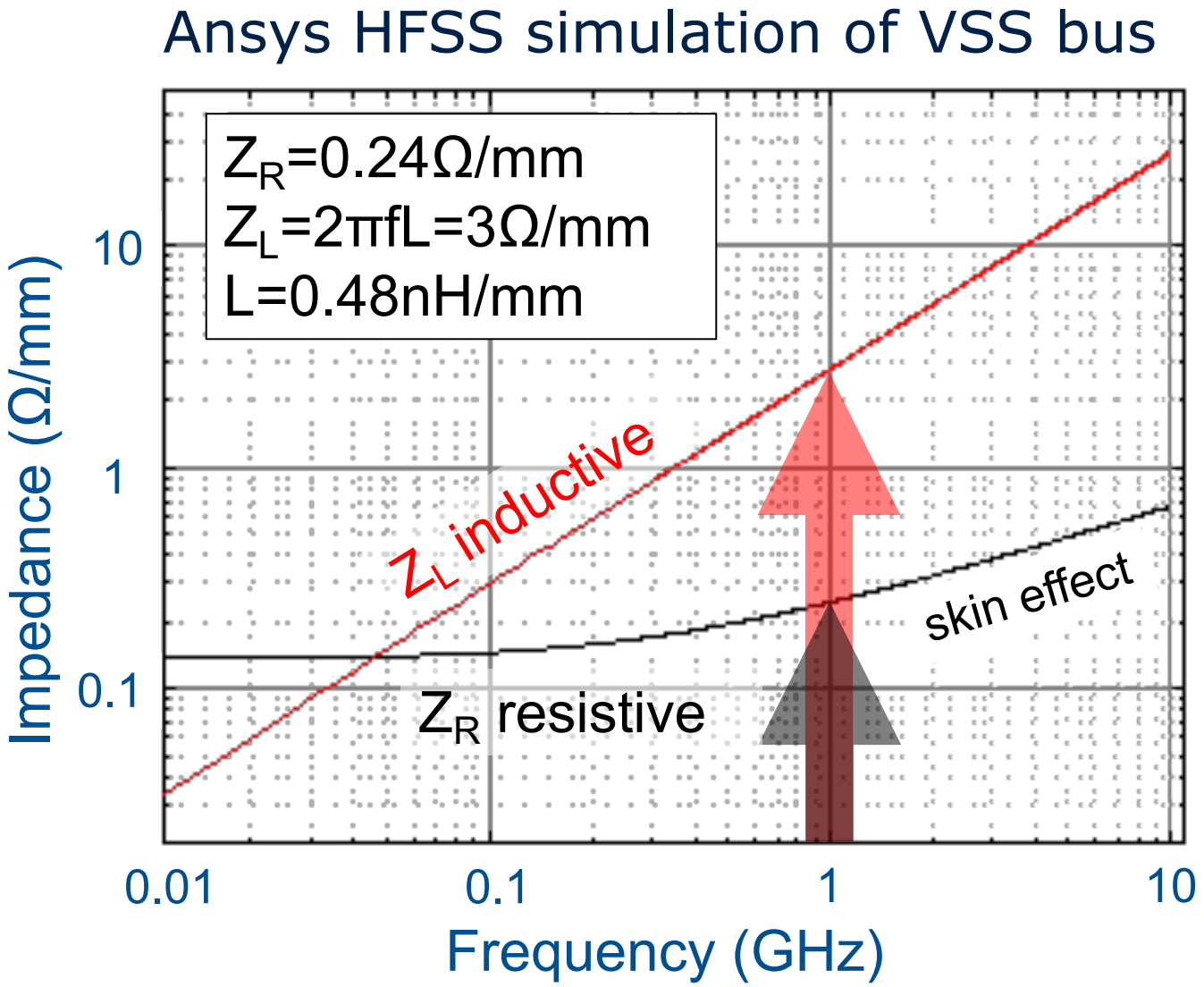


- CDM center frequency around 1 GHz
- Input parameter for inductive contribution of bus line

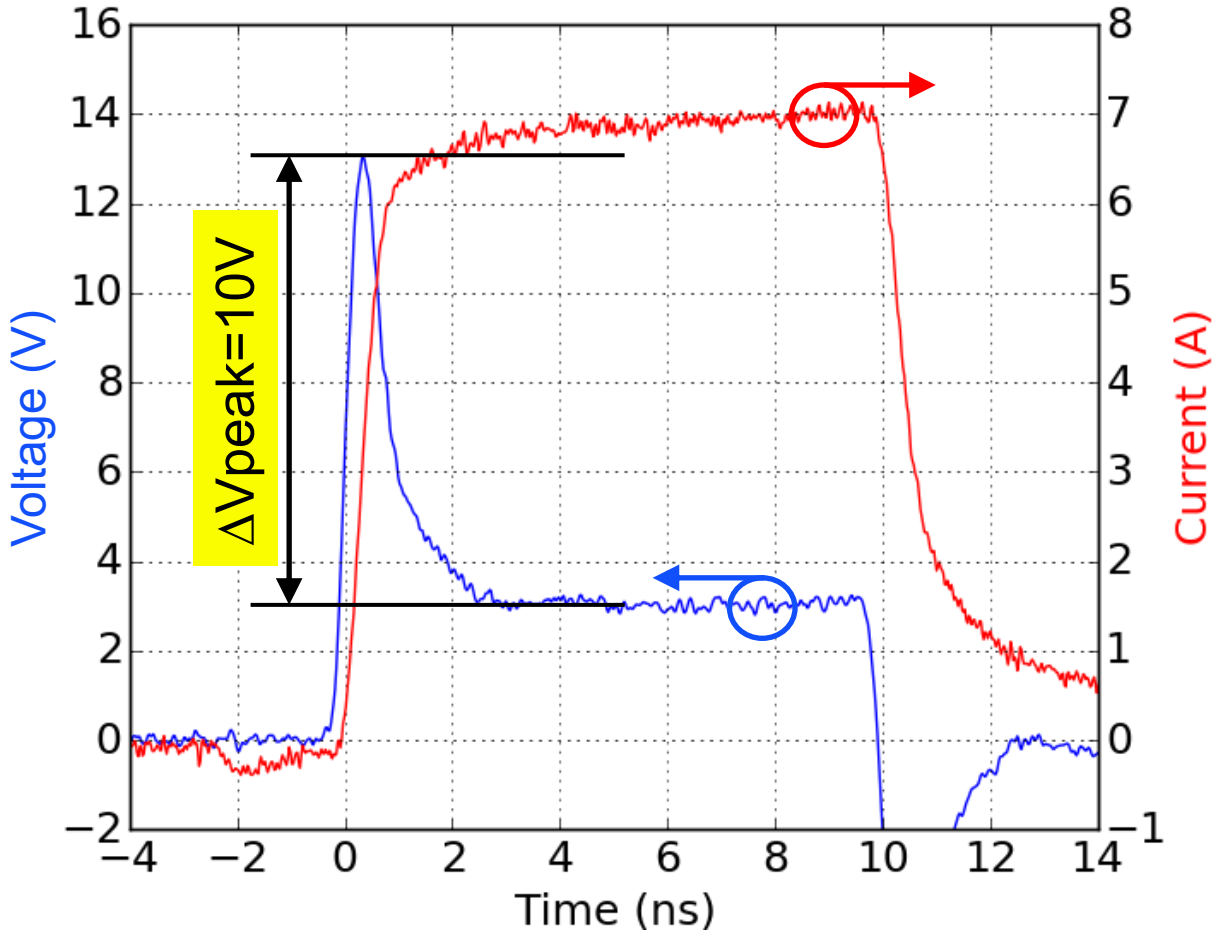
CDM Case Study - Bus Line Inductance

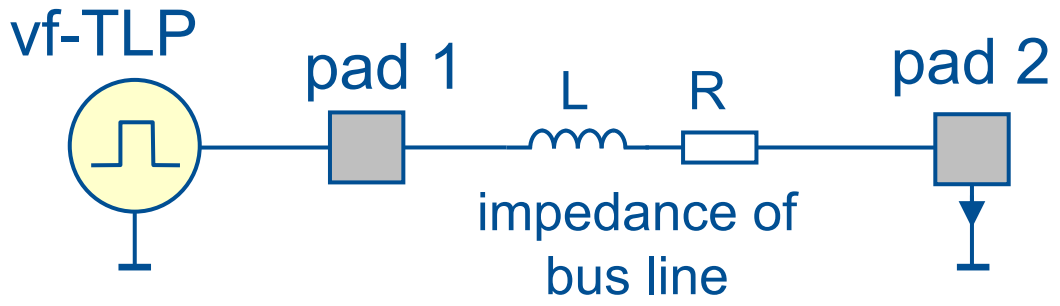


- Ohmic resistance of top metals has decreased with technology advancement
- Bus lines became narrower → higher inductance
- CDM frequency range: $Z_L > Z_R$



CDM Case Study - Bus Line Inductance





- Experimental demonstration of impact of bus line inductance:
- L=2mm
- 600ps risetime pulse, 7A current
- Inductive voltage peak ΔVpeak=10V much larger than resistive voltage drop of 3V
- Voltage transient can be experienced by domain interfaces!

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- CDM Case Study
  - Bus Line Inductance
  - Modified Tool Setup
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Extended Methodology: Automated Inductance Extraction

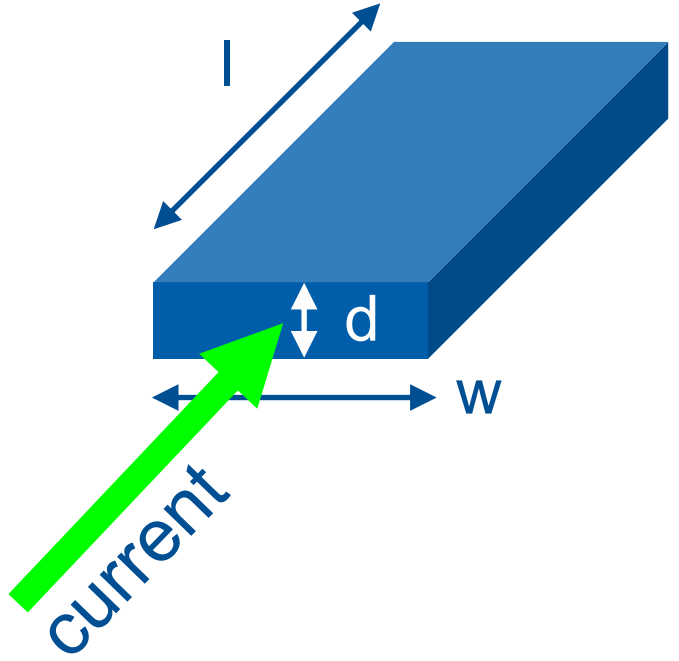
- Inductance of straight conductor [Kalantarov]:

$$L = \frac{\mu_0 l}{2\pi}\left(\ln\frac{2l}{d+w} + \frac{1}{2}\right) \quad for \quad l \gg d, w$$

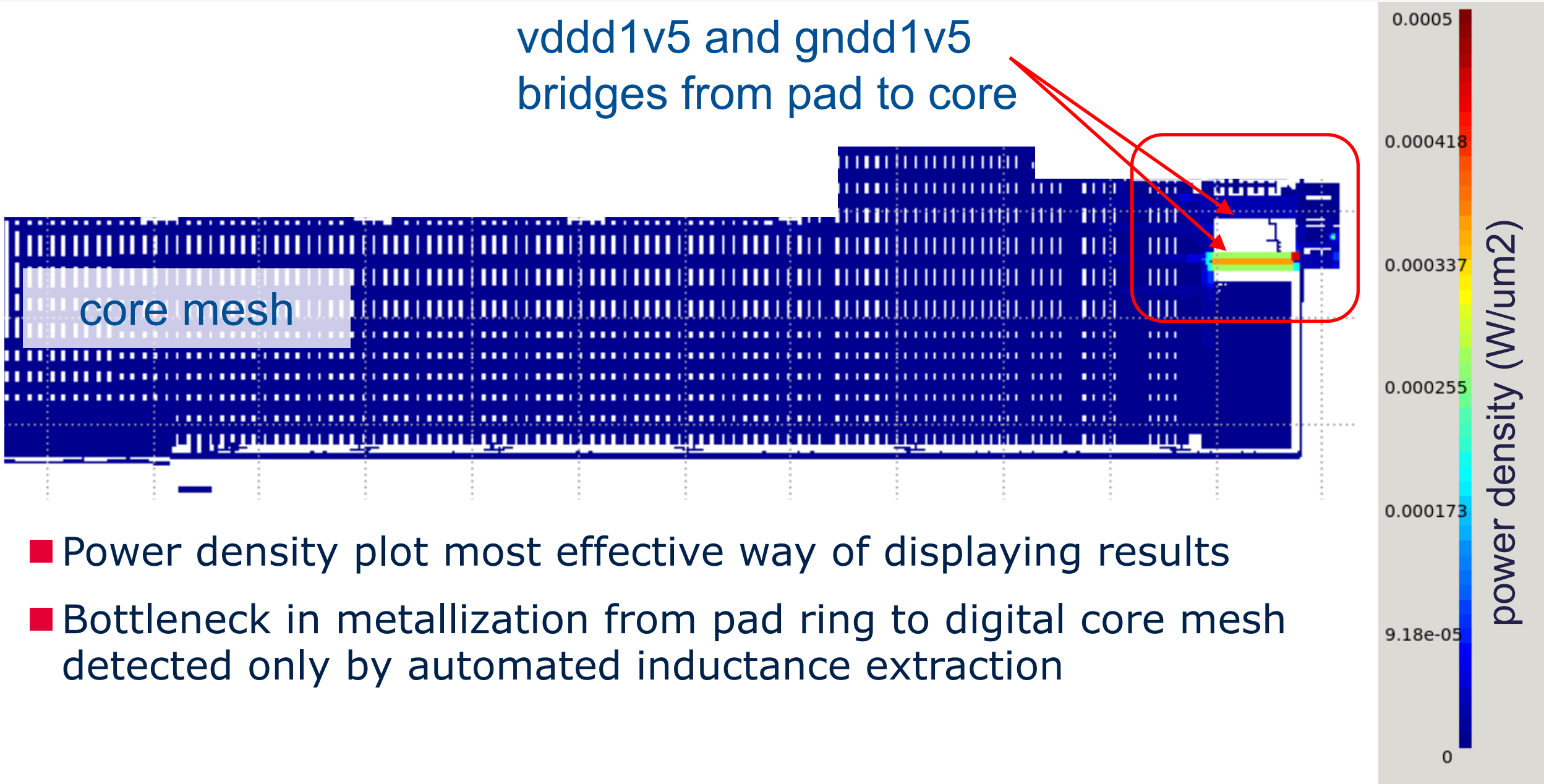
- Implementation in ESRA-CDM to account for inductive effects in addition to ohmic effects

$$V = \sqrt{V_{ind}^2 + V_{res}^2} \quad with \; V_{ind} = 2\pi f L I_{path} \; and \; V_{res} = R I_{path}$$

- Manual or automated application to long wires
- Quasi-static approach, almost no impact on tool run time

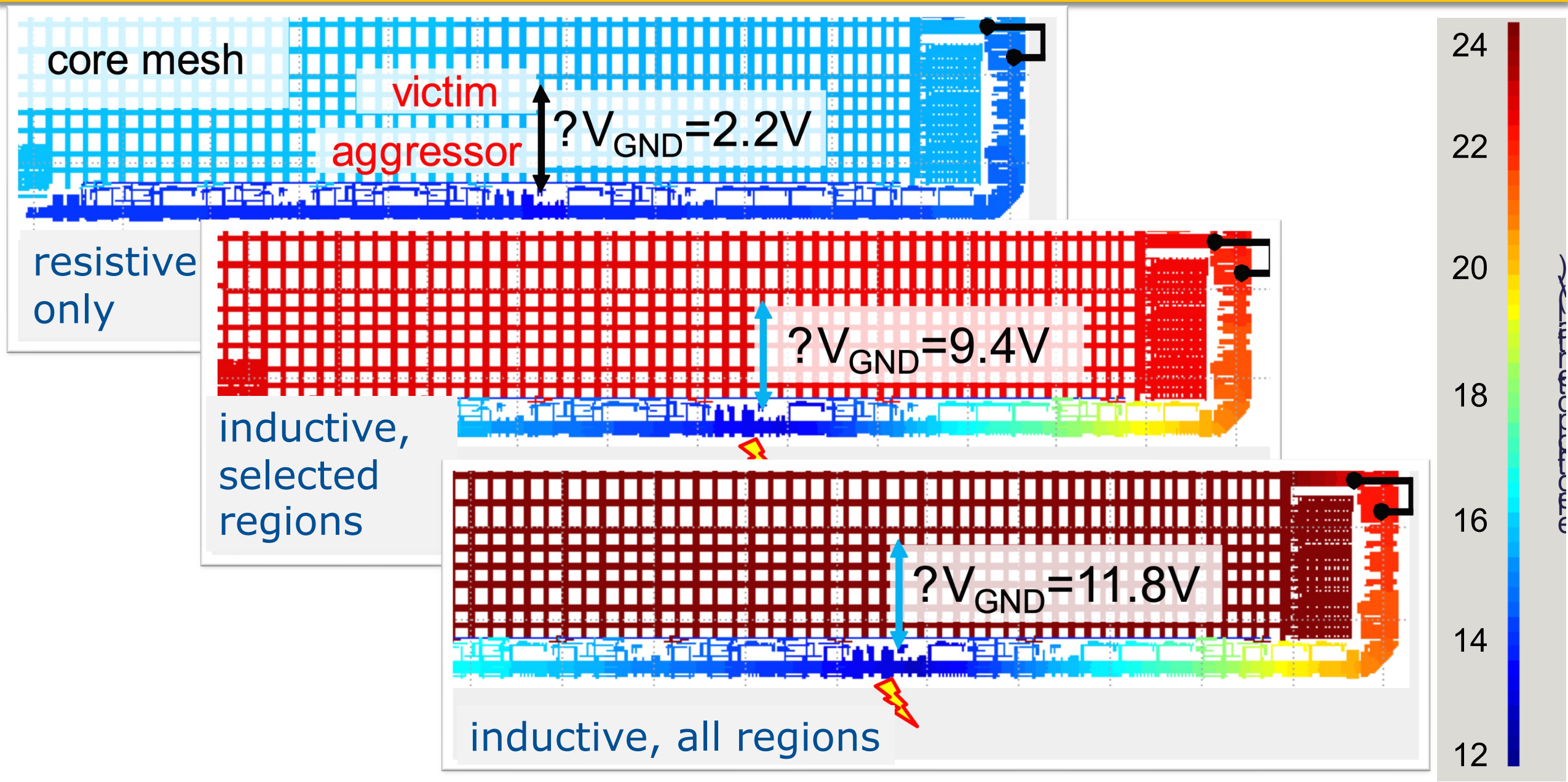


Localization of Highly Inductive Regions

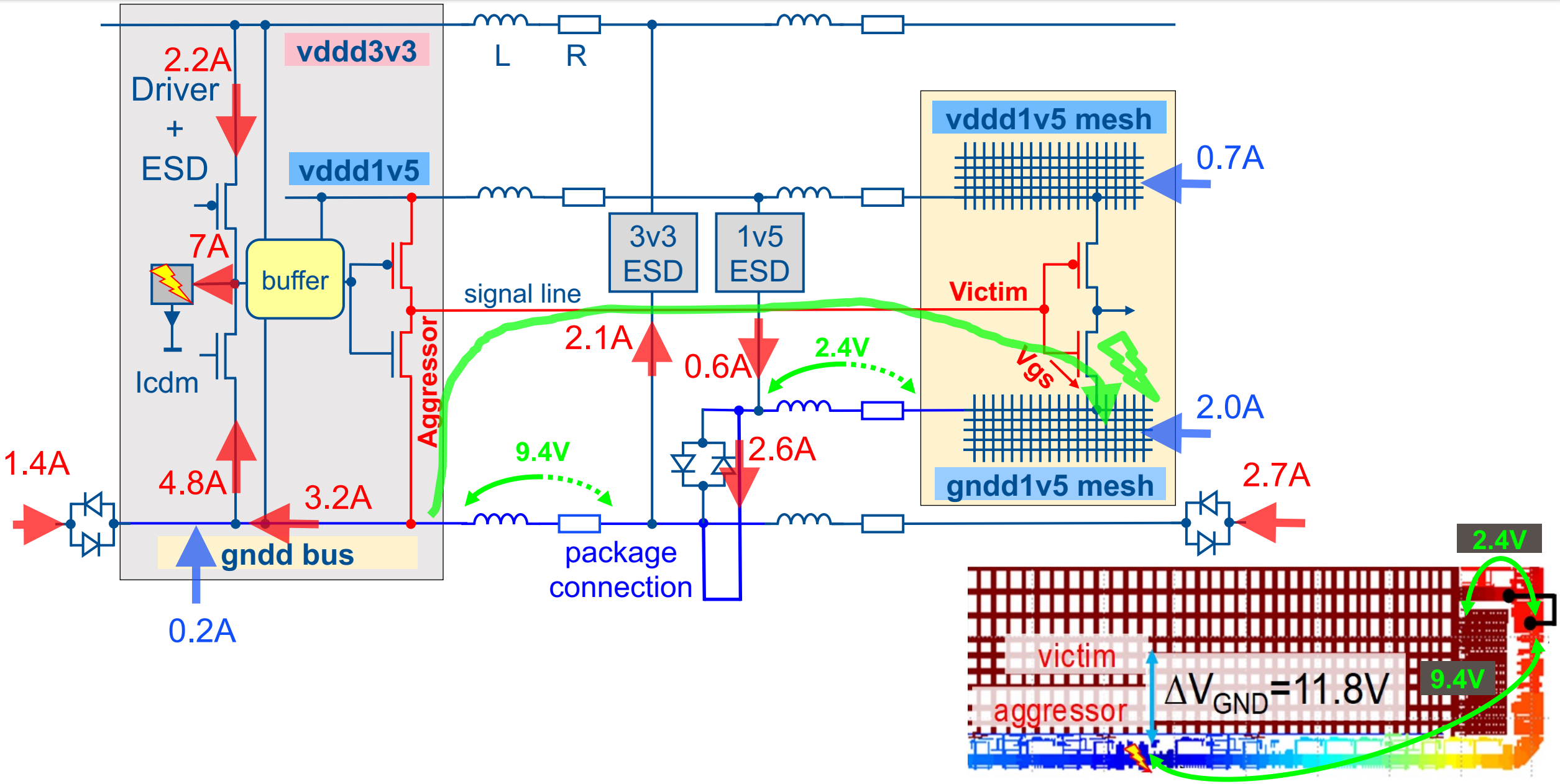


- Power density plot most effective way of displaying results
- Bottleneck in metallization from pad ring to digital core mesh detected only by automated inductance extraction

Tool Enhancements for Treatment of Inductance



Analysis of Intra-Domain Issue on Chip Level (2)



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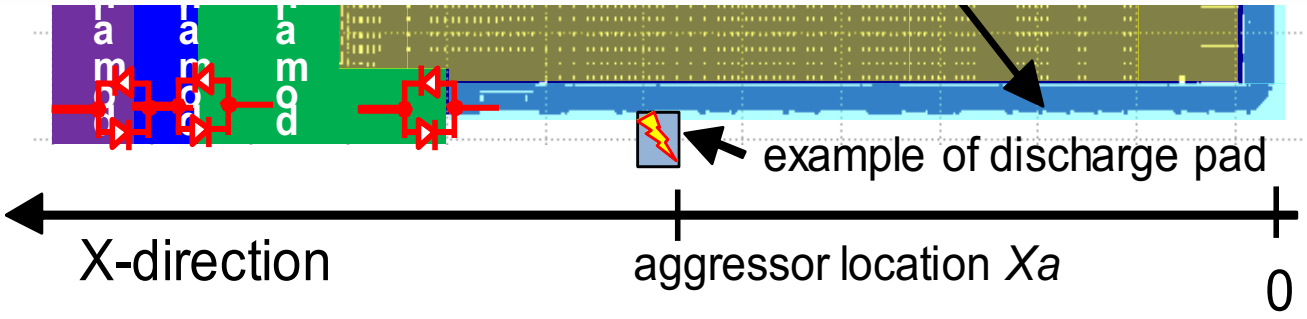


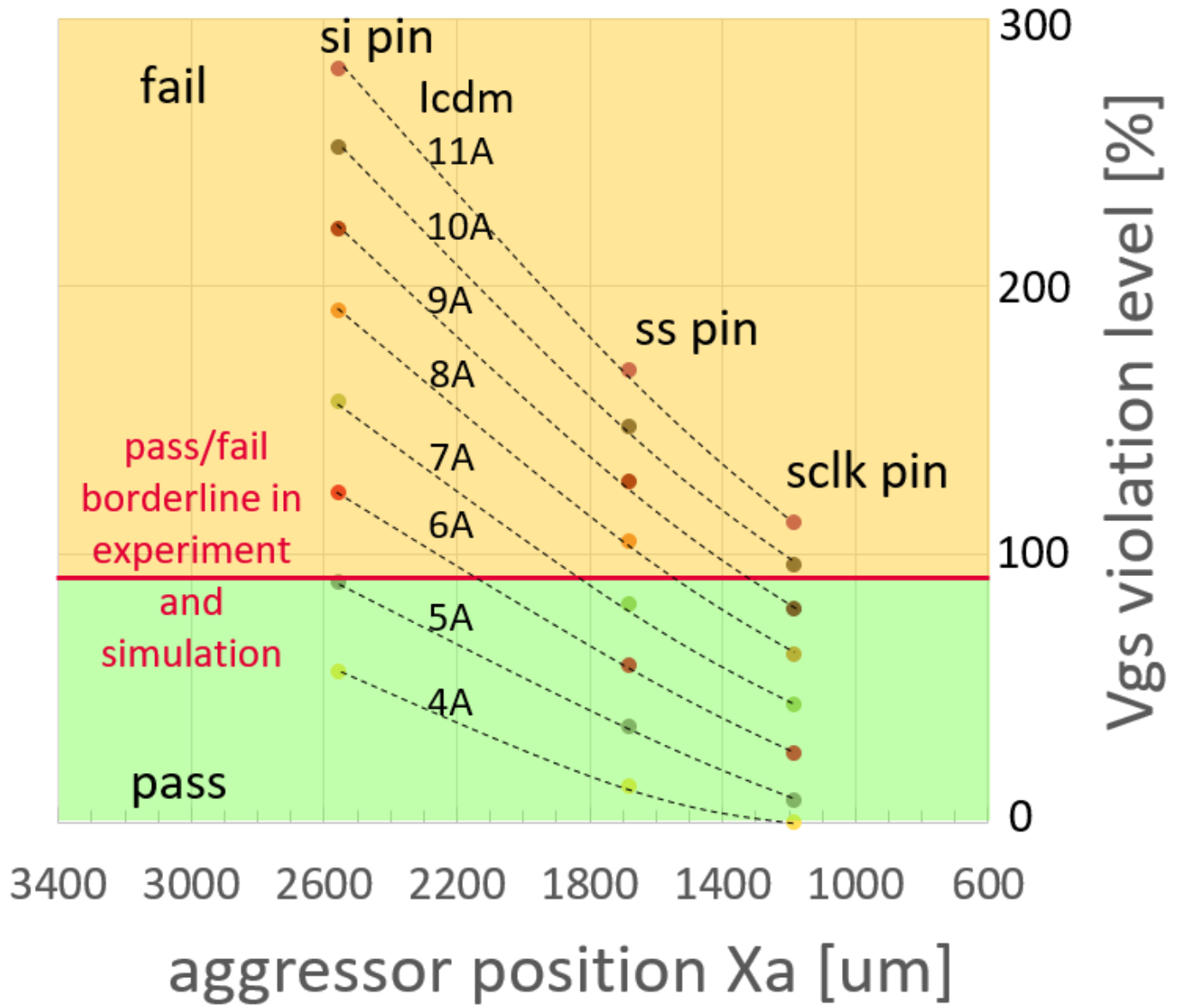
- Pad-specific ESD robustness
- Correlation CCTLP vs ESRA

pin	Xa (um)	CCTLP-experiment							
		4A	5A	6A	7A	8A	9A	10A	11A
sclk	1182	pass	pass	pass	pass	pass	n/a	fail	n/a
ss	1682	pass	pass	pass	pass	fail	n/a	fail	n/a
si	2557	pass	pass	fail	fail	fail	n/a	fail	n/a

pin	Xa (um)	Vgs violation by ESRA (in % above 6.0V)							
		4A	5A	6A	7A	8A	9A	10A	11A
sclk	1182	0	8	26	44	63	80	96	112
ss	1682	13	35	59	81	105	127	147	169
si	2557	56	90	123	157	191	221	252	281

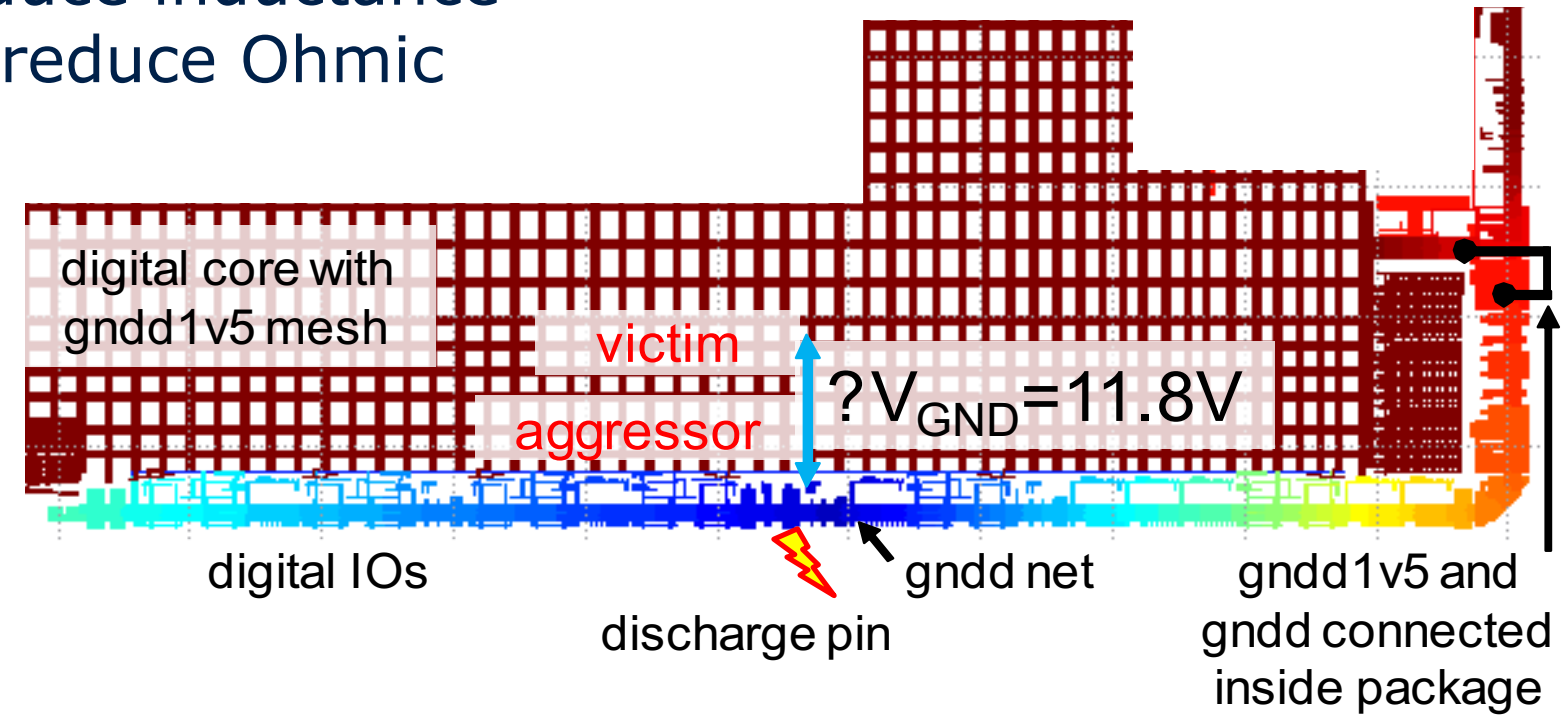
Comparison of CDM Levels: Tool vs. Experiments

- Correlation between failure current and 90% Vgs violation
- Why 90%?
  - 0% = design limit of 6.0V
  - 90% above limit = 11.4V
  - Actual failure level > design limit
  - Voltage at victim: RC delays, top portion of voltage pulse contributes to actual gox breakdown
- Conservative Vgs design limit still recommended, some relaxation possible



Design Improvements

- Small local metal straps between
  - vddd1v5: bus ←→ core mesh
  - gndd1v5: bus ←→ core mesh
- Local interface protection at the receivers
- Metal reinforcements: reduce inductance prevailing over efforts to reduce Ohmic resistances!



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Conclusions

- CDM failure observed despite adherence of existing design rules
- Gate oxide characterization down to nano-second range: careful relaxation of limits possible
- Accounting for inductances in the layout:
  - Focus on inductances which are part of CDM discharge path
  - Several relevant locations detected: pad ring and core hook-up
- Intra-domain problem verified with extended tool methodology
  - Signal lines from pad ring to core transmit large voltage drop; failure of receiver(s)
  - Explanation of CDM robustness depending on pad location and bus length
- Inductance of busses matters because of excessive CDM voltage drops
- Technology trend: inductance dominates over resistive impedance $Z_L > Z_R$